

**WHAT IS CLAIMED IS:**

- 1     1.     A method for verifying scan chain equivalency between two representations of a  
2     circuit design having at least one scannable state element, at least one scan-out and at  
3     least one output pin, comprising:  
4         for each representation of the circuit design, loading each scannable state element  
5             with a symbolic expression that characterizes a logical location of said  
6             scannable element in the circuit design; and  
7         for each representation of the circuit design, performing a scan shift operation to  
8             verify the contents of each scannable state-element at said scan-out and  
9             output pins of the design.
- 1     2.     The method of claim 1, wherein the two representations of a circuit design  
2     comprise a switch-level netlist and an RTL netlist.
- 1     3.     The method of claim 1, wherein the two representations of a circuit design  
2     comprise a transistor level implementation and a behavioral level description.
- 1     4.     The method of claim 1, wherein the two representations of a circuit design  
2     comprise RTL and schematic models of a memory circuit.
- 1     5.     The method of claim 1, wherein the two representations of a circuit design  
2     comprise a first RTL model of a storage circuit and a second RTL model of a storage  
3     circuit.
- 1     6.     The method of claim 1, wherein the two representations of a circuit design  
2     comprise a SPICE-level netlist and a gate level description.
- 1     7.     The method of claim 1, wherein said loading of each scannable state element with  
2     a symbolic expression comprises simulating said circuit design in a functional mode for a

3 first minimum threshold number of cycles by applying symbolic expressions to at least a  
4 first input for said circuit design.

1 8. The method of claim 7, wherein said first minimum threshold number comprises  
2 the maximum sequential depth of all scannable state-elements on all paths from all  
3 primary inputs in said circuit design.

1 9. The method of claim 1, wherein said loading and performing steps are  
2 implemented with a symbolic simulator to check scan chain equivalency with respect to  
3 complete scan chain connectivity from primary input to primary output, logical location  
4 of all scannable state elements, scan chain length and scan chain order.

1 10. The method of claim 1, wherein said loading and performing steps are  
2 implemented with a symbolic simulator to obtain complete coverage.

1 11. The method of claim 1, wherein said scan shift operation comprises simulating a  
2 sequence of scan clocks equal to a multiple of the number of scannable state-elements in  
3 the circuit design.

1 12. An article of manufacture having at least one recordable medium having stored  
2 thereon executable instructions and data which, when executed by at least one processing  
3 device, cause the at least one processing device to verify equivalency of a scan chain  
4 design comprising at least a first scannable memory-element by:

5 storing a first representation of a scan chain design;  
6 storing a second representation of the scan chain design;  
7 symbolically simulating the scan chain design by applying symbolic inputs to  
8 inputs in the first and second representations of the scan chain design;  
9 performing a scan shift on the first and second representations to verify the  
10 contents of each scannable memory element at an output of the scan chain  
11 design.

1 13. The article of manufacture defined in claim 12, wherein the instructions and data  
2 cause the at least one processing device to symbolically simulate the scan chain design by  
3 loading each scannable memory element in the scan chain design with a symbolic  
4 expression that is characteristic of a logical location for that scannable memory element.

1 14. The article of manufacture defined in claim 12, wherein the first representation  
2 comprises an RTL level description of the scan chain design, and the second  
3 representation comprises an schematic level description of the scan chain design.

1 15. The article of manufacture defined in claim 12, wherein the instructions and data  
2 cause the at least one processing device to symbolically simulate the scan chain design by  
3 symbolically simulating the scan chain design in functional mode for a threshold number  
4 of cycles, where the threshold number equals the maximum of all sequential depths of all  
5 scannable memory elements on all paths from all primary inputs in the scan chain design.

1 16. The article of manufacture defined in claim 15, wherein the instructions and data  
2 cause the at least one processing device to perform scan shifting after the scan chain  
3 design has been symbolically simulated in function mode to thereby verify the contents  
4 of each scannable memory element at a scan-out pin of the design.

1 17. The article of manufacture defined in claim 12, wherein the scan chain design  
2 comprises at least a portion of microprocessor circuitry.

1 18. The article of manufacture defined in claim 12, wherein the scannable memory  
2 element comprises a flop-flop.

1 19. A scan chain integrated circuit, comprising:  
2 a plurality of circuit components for processing data signals in accordance with a  
3 timing sequence controlled by at least one clock signal; and  
4 one or more scannable state-elements for use in performing DFT testing on the  
5 plurality of circuit components;  
6 wherein the design of said scan chain integrated circuit is verified by:

- 7 (a) generating a first description of the scan chain integrated circuit comprising a
- 8 representation at a first level of abstraction;
- 9 (b) generating a second description of the scan chain integrated circuit
- 10 comprising a representation at a second level of abstraction;
- 11 (c) loading each scannable state-element in the first and second descriptions with
- 12 a unique symbol characterizing the logical location of the scannable state-
- 13 element in the scan chain integrated circuit design;
- 14 (d) symbolically simulating the first and second descriptions in functional mode;
- 15 and
- 16 (e) performing a scan shift on the first and second descriptions to verify
- 17 equivalency of the first and second descriptions by checking the contents
- 18 of said scannable state-element at a first and second output of said first
- 19 and second descriptions.

1 20. The scan chain integrated circuit of claim 19, wherein the first description  
 2 comprises a switch-level netlist description, and the second description comprises an  
 3 RTL netlist.